Omar Radwan, PE

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Education

University of Southern California - USC Viterbi School of Engineering *CA*
M.S. Computer Engineering *2022*

University of California, Los Angeles - UCLA Henry Samueli School of Engineering *CA*
B.S. Computer Engineering *2021*

Employment

Apple Inc.
SEG GPU Physical Design Engineer *2023 - Present*

California State University Fresno, Department of Computer Science
Graduate Computer Science Faculty *January 2023 - May 2023*
- Member of the Fresno State Graduate Computer Science Department faculty
- Instructor for CSCI200: Introduction to Research, teaching first-semester graduate students on the computer science research processes, introductory academic writing, presentation skills, proposal writing, and how to perform research and literary review
- Instructor for CSCI201: Computer Science Colloquium, building on CSCI200 to further examine the peer review process, professional development, and practitioner and conference paper analysis

Apple Inc.
SEG GPU Physical Design Engineering Intern *May 2022 – August 2022*
- Performed physical design verification including DRC, LVS, ERC, and ANT on active GPU projects
- Triaged verification results to diagnose systemic issues and provided wider physical design team with set of actionable issues to resolve before signoff
- Improved internal physical verification infrastructure to reduce turn-around-time for resolution of macro placement and floorplanning issues

Mentor Graphics (Now Siemens EDA)
Research and Development Intern - SRC Sponsoree *September 2020 - June 2021*
- Exposed to advanced functionality and use of Calibre Design Suite, including Calibre RVE, PERC, DFM, nmDRC, and nmLVS VLSI tool-chains
- Worked with greater team to develop performance enhancements and features for the nmLVS and PERC tools
- Used PMD to generate analysis of Calibre suite detailing and differentiating legacy modules from more modern components, and created a plan of action for modernizing Calibre software base
- Utilized LCov to debug legacy Calibre components by incorporating in-house regression tests for code coverage analysis
- Created a Python-based code coverage utility with IDE plugins to automate regression testing for Calibre nmLVS, nmDRC, PERC, and DFM on batch processing network

Licenses and Professional Registrations

California Board for Professional Engineers, Land Surveyors, and Geologists (BPELSG)
Professional Engineer - Electrical Engineer License #: 25324

United States Patent and Trademark Office (USPTO)
Patent Agent - Registration #: 80626

Research Projects and Publications

Discrete Search in Heterogeneous Integer Spaces for Automated Choice of Parameters using Correct-by-Construction Methods
Radwan, Omar, et al. 'Discrete Search in Heterogeneous Integer Spaces for Automated Choice of Parameters Using Correct-by-Construction Methods'. ArXiv [Eess.SY], 2023, arXiv.

Low-Power Network-Native Hardware Encryption for IoT
Implemented a RISC-V hardware-accelerated IoT SoC on NetFPGA (Formerly Patent Pending - USPTO Application # 63/346,853)
- Designed pipelined multi-core low-power RISC-V SoC with network FIFO and RISC-V RV32i support
- Created RISC-V assembler with macro-op support and processor communication suite for use with 32-bit instruction set and 64-bit register-file/datapath for RV32i ISA subset
- Produced low-power novel hardware implementation of Speck 128-bit security cipher and integrated it into RISC-V processor with 2x order of magnitude performance increase over software implementation with 500Mbps on-the-fly encryption
- Used the open-source OpenROAD ASIC design flow to create Skywater 130nm physical implementation that meets all required signoff targets for fabrication

Skills

Hardware Languages	Verilog, VHDL, Migen
Programming Languages	Python, C, C++, Tcl, UNIX Shell (tcsh, bash, zsh), Assembly (ARM, RISC-V), Matlab
Hardware Design Tools	Cadence Innovus, Virtuoso; Synopsys PrimeTime, DC; Siemens Calibre; Xilinx ISE, Vivado; OpenROAD; KiCAD PCB
Development Environments	Red Hat Linux/CentOS, Ubuntu, AWS

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